

**A High Performance IC Chip having Discrete Decoupling Capacitors
Attached to its IC Surface**

This application claims priority to U.S. Provisional Patent Application serial number 60/455154, filed on March 17, 2003, which is herein incorporated by reference.

Related Patent Application

Related U.S. Patent Application Serial number _____ (MEG02-014), to _____, filed on _____.

Background of the Invention

Field of the Invention

This invention relates to structures and methods of assembly of integrated circuit chips. More particularly, this invention relates to mounting discrete decoupling capacitors on the surface of IC chips.

Description of the Related Art

Current wirebonding packages, for example, ball grid arrays (BGA), suffer from power/ground noise due to the inductance of wirebonds and package leads. This issue becomes severe in advanced chips performing at high frequency and low voltage. Flip chip packages are now used to reduce the inductance from wirebonds. However, the industry infrastructure for flip chip packages is not so mature as wirebonding packaging. Most importantly, flip chip packages require high density substrates which are much more expensive than wirebonding substrates. Wirebonds act as the fan-out metal lines; therefore the routing density on substrates is relaxed. Other approaches attempt to solve the power/ground problem by building on-chip decoupling capacitors using thin-film IC processes for the wirebonding packages. However, the built-in capacitors cannot provide large enough magnitude capacitance for decoupling purposes.

U.S. Patents 6,303,423 and 6,515,369, both by M.S. Lin, teach methods and structures of mounting a discrete component on the surface of an IC chip. Related Patent Application serial number _____ (MEG02-014) discloses methods of making both solder bumps and wirebond pads on the same wafer. U.S. Patents 6,495,442 and 6,383,916 to M.S. Lin et al disclose a post-passivation interconnection process. U.S. Patents 6,184,574 and 6,504,236 both to Bissey disclose an integrated circuit lead frame with capacitors formed on the

lead frame and bonded to the bottom surface of the chip for decoupling purposes.

Summary of the Invention

An object of this invention is to provide discrete decoupling capacitors mounted on the surface of an IC chip.

Another object of this invention is to provide a method for mounting discrete decoupling capacitors on the surface of an IC chip.

A further object is to provide a wirebonding package for high performance and low power IC chips by adding surface mounted decoupling capacitors.

A still further object is to attach surface mounted decoupling capacitors to wirebonds through IC metal lines under passivation.

Another object is to attach surface mounted decoupling capacitors to wirebonds through post-passivation metal lines above the passivation layer.

Yet another object of the invention is to connect surface mounted decoupling capacitors to power/ground buses under the passivation layer.

In accordance with the objects of the invention, a high performance integrated circuit chip is disclosed comprising semiconductor device structures in and on a substrate, a plurality of levels of interconnection lines and interlevel dielectric materials overlying and connecting the semiconductor device structures wherein at least one contact pad is interconnected, a passivation layer overlying the plurality of levels of interconnection lines and interlevel dielectric materials, wirebonds formed overlying the passivation layer and connected to at least one contact pad, and at least one discrete decoupling capacitor mounted on a solder wettable surface over the passivation layer wherein the discrete decoupling capacitor is connected to wirebonds and to power/ground buses.

Also in accordance with the objects of the invention, a method of fabricating a high performance integrated circuit chip is achieved. Semiconductor device structures are formed in and on a substrate. A plurality of levels of interconnection lines and interlevel dielectric materials are formed overlying and connecting the semiconductor device structures wherein a topmost level of the interconnection lines includes at least one contact pad. A passivation layer is deposited overlying the plurality of levels of interconnection lines and interlevel dielectric materials. Vias are opened through the passivation layer to the contact pad. Metal lines are formed in the vias and overlying the passivation layer. Wirebonds are formed on the metal lines. Solder pads are formed on the metal lines adjacent to the wirebonds. At least one discrete

decoupling capacitor is mounted on the solder pads wherein the discrete decoupling capacitor is connected to wirebonds and to power/ground buses.

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Brief Description of the Drawings

Fig. 1 shows a cross-sectional view of a preferred embodiment of the present invention.

Fig. 2 shows a cross-sectional view of a first preferred embodiment of the present invention in which the decoupling capacitors are connected to metal lines underlying the passivation layer.

Fig. 3 shows a cross-sectional view of a second preferred embodiment of the present invention in which the decoupling capacitors are connected to post-passivation metal above the passivation layer.

Fig. 4A shows a cross-sectional view of a first alternative to the second preferred embodiment of the present invention in which the wirebonds are connected to the underlying fine-line metal line.

Fig. 4B shows a cross-sectional view of a second alternative to the second preferred embodiment of the present invention in which the wirebonds are connected to the decoupling capacitors through the underlying fine-line metal line.

Figs. 5 through 8 show cross-sectional views of additional alternatives in the second preferred embodiment of the present invention.

Detailed Description of the Invention

In the present invention, discrete decoupling capacitors are mounted on the surface of an IC chip. Since a discrete capacitor can provide the capacitance of the magnitude μF , the attached capacitors can serve as the local power reservoir to decouple the external power ground noise caused by wirebonds, packages, and other system components. It will be understood by those skilled

in the art that the present invention should not be limited to any of the examples shown, but can be extended and applied to any kind of IC chip design.

Referring now to Fig. 1, there is shown an example of a preferred embodiment of the present invention. Semiconductor substrate 10 is shown. Transistors and other devices, not shown, are formed in and on the semiconductor substrate 10. Dielectric layer 12 is formed over the substrate 10. Conductive interconnect lines 11 are formed within the dielectric layer connecting to devices formed in and on the substrate, not shown. Layers 14 represent the plurality of metal and dielectric layers formed in a typical integrated circuit. Two layers 14 are shown in Fig. 1, including metal interconnects 13. Multiple layers of dielectric materials may be included in layers 14. More than two layers 14 may be present. Overlying these layers 14 are points of contact 16 that will be connected to surrounding circuitry. Passivation layer 18 is formed over the contacts 16. The passivation layer may comprise silicon oxide or silicon nitride or a composite of these materials. The passivation layer prevents the penetration of mobile ions, such as sodium ions, moisture, transition metals, such as gold, silver, copper, and so on, and other contaminations. The passivation layer is used to protect the underlying devices, such as transistors, polysilicon resistors, poly-to-poly capacitors, and fine-line metal interconnections. Now, connection is to be made to the next level of packaging. Wirebonding is to be used in the connection. Discrete decoupling capacitors are mounted on the surface of the IC chip. In one preferred embodiment of the invention, the

decoupling capacitors are connected to the wirebond through IC metal lines under the passivation layer. Discrete capacitors provide optimized parameters and can be mounted close to the circuits, which offer system-on-chip performance and minimizes parasitics. The post-passivation process of the present invention allows for the selection of discrete capacitor design parameters that result in reduced resistance of the discrete capacitor.

Referring now to Fig. 2, there is shown the first preferred embodiment of the invention. A typical discrete decoupling capacitor 38 is shown. This commercially available discrete capacitor has already been coated with solder, not shown, at both ends, terminals or electrodes 34.

In the first preferred embodiment of the invention, the decoupling capacitors are connected to the wirebond through IC metal lines under the passivation layer 18. Wirebonds 26 and 28 are shown. The wirebonds are bonded to metal segments Vdd and Vss in the top layer of metal underlying passivation layer 18. To facilitate the reader's review of the process, the wires have been arranged in a specific manner in the figures. The wirebond on the left 26 is connected to Vdd and the wirebond on the right 28 is connected to Vss. It will be understood that this specific manner of connection is not essential and may be changed without departing from the spirit and scope of the invention.

Decoupling capacitor 38 is also connected to the same metal segments Vdd and Vss, as shown.

Solder pads 31 are formed to connect the capacitor electrodes 34 to the metal segments Vdd and Vss. The capacitor 38 serves as a local power reservoir to decouple the external power ground noise caused by the wirebonds 26 and 28 and other system components. A decoupling capacitor is connected in association with each of at least two wirebonds.

The capacitors are mounted on the silicon wafers, for example, using standard Surface Mount Technology (SMT) as in the Printed Circuit Board industry. The commercially available discrete capacitors have been already coated with solder at both ends (terminals or electrodes). Therefore, on the IC wafer, the solder pads 30 are prepared with a solder wettable surface. For example, solder cream can be printed on the IC pads. Solder 31 is shown in Fig. 2 on the solder pads 30.

Alternatively, surface mountable pads may be created. The surfaces of the solder pads 30 are finished with a solder wettable material such as solder, gold, or copper by electroplating, electroless plating, or sputtering. Furthermore, a diffusion barrier metal, not shown, is required under the solder wettable metal to prevent intermetal diffusion between the solder and the pad metal.

The capacitor 38 is surface-mounted on the chip, as shown, and serves as a buffer between the underlying electrical devices and the outside circuit. Thus, the capacitor has a decoupling function when acting as a power reservoir, so that when one of the underlying semiconductor devices suddenly requires a relatively large electric current, the capacitor 38 can immediately supply power to the device. Moreover, the capacitor 38 can be provided with a high electrical capacity so that a sudden voltage drop between the power bus and the ground bus can be prevented. Furthermore, when a relatively large electrical charge flows into the chip, the capacitor 38 acts as a buffer to prevent damage to underlying semiconductor devices. Alternately, the capacitor can be used to isolate an attached circuit from ground noise.

In a second preferred embodiment of the invention, the decoupling capacitors are connected to the wirebond through post passivation metal lines above the passivation layer. Referring now to Fig. 3, there is shown an example of the second preferred embodiment of the invention.

The device and metal interconnect layers are as shown in Figs. 1-2. The topmost metal layer is 16. Passivation layer 18 has been formed over this metal layer, as described above. The passivation layer prevents the penetration of mobile ions, such as sodium ions, moisture, transition metals, such as gold, silver, copper, and so on, and other contaminations. The passivation layer is

used to protect the underlying devices, such as transistors, polysilicon resistors, poly-to-poly capacitors, and fine-line metal interconnections.

Now, the post-passivation metallization, formed of, for example, copper or gold, is to be formed. The post-passivation metallization is described in co-pending U.S. Patent Application MEG02-018, serial number 10/445,560, filed May 27, 2003, and herein incorporated by reference. Openings are made through the passivation layer 18 to form thick metal lines 23.

A post-passivation dielectric layer 25 is deposited over the thick metal lines 23. Preferably, this layer 25 is polyimide having a thickness of between about 2 and 150 microns, depending on electrical design requirements. Alternatively, the layer 25 could be made of benzocyclobutene (BCB), a porous dielectric material, parylene, or an elastomer, for example.

Now, openings are made to the thick metal lines 23 for wirebonds 26 and 28. Openings are made through the post-passivation dielectric layer 25 to the metal lines 23 for connecting the decoupling capacitor 38. Connection is as described above in the first embodiment.

Wirebonds may be made directly to the post passivation metallization 23 if a thick layer of gold (greater than about 1 micron) is used for the metallization. An underbump metallization (UBM) layer is required for solder bumping to gold

less than 1 micron thick, or to copper. If a wirebond is to be made to copper, a layer of nickel, then a layer of gold are formed over the copper.

In Fig. 4A, the thick metal layer 23 and post-passivation dielectric layer 25 have been patterned to underlie the capacitor area. Wirebonds 26 and 28 are formed to the metal line 16 rather than to the thick metal lines 23. In Fig. 4B, the decoupling capacitor 38 is connected to the wirebonds 26 and 28 through the metal line 16.

In Fig. 5, for example, gold pads 40 are formed through openings in the passivation layer 18 to the metal lines 16 under the passivation layer. The wirebonds 26 and 28 are connected to the gold pads.

The decoupling capacitor 38 is mounted on the surface of the IC chip. Solder pads must be created for the mounting process. Co-pending U.S. Patent Application serial number _____ (MEG02-014) describes a process for forming both gold wirebond pads and solder pads on the same wafer.

In an alternative illustrated in Fig. 6, the wirebonds 26 and 28 are made directly to the metal line 23 without an intervening post-passivation dielectric layer. The capacitor 38 is also mounted directly on the metal line 23 by solder 31. A solder bonding metal, not shown, can be provided between the solder 31 and the metal lines 23.

In a third preferred embodiment of the present invention, a thick post-passivation dielectric layer is formed underlying the thick metal lines. As shown in Fig. 7, a thick post-passivation dielectric layer 21, such as polyimide, is deposited over the passivation layer 18. Openings 70 are made through the post-passivation dielectric layer 21 and the passivation layer 18 to the metal lines 16. Thick metal lines 23 are formed to contact the metal lines 16.

Now, a second thick post-passivation dielectric layer 25, such as polyimide, is deposited over the thick metal lines 23. Now, openings are made in the second post-passivation dielectric layer 25 to the thick metal lines 23. Wirebonds 26 and 28 are made within these openings. Similarly, openings are made to the thick metal lines 23. The capacitor 38 is connected to the metal lines 23 with solder 31.

Fig. 8 illustrates a further alternative in which two layers of thick metal lines are formed in a post-passivation process. The first thick metal lines 23 are formed overlying the passivation layer 18 and connected to the interconnection lines 16 through openings in the passivation layer 18. A first post-passivation dielectric layer 25 is deposited overlying the first thick metal lines. Second thick metal lines 43 are formed overlying the first post-passivation dielectric layer and connected to the first thick metal lines through openings in the first post-passivation dielectric layer. A second post-passivation dielectric layer 45 is

deposited over the second thick metal lines. Wirebonds 26 and 28 are formed through openings in the second post-passivation dielectric layer 45 to the second thick metal lines 43. Decoupling capacitor 38 is connected to the interconnection lines 16 through openings in the second post-passivation dielectric layer 45 to the second thick metal lines 43.

While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is: